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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,387	09/27/2001	Jason E. Cosky	42390.P11979	2940

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,387	COSKY ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *03 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-52,54-57,59 and 60* is/are rejected.

7)☒ Claim(s) *53 and 58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on January 3, 2005.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 44, 47-48, 51, 54-56 and 59-60 are rejected under 35 U.S.C. 102(b) as being anticipated by Maruyama (JP 05120128).

Regarding claims 44 and 47, Maruyama discloses a memory element directly (Figure 1, Reference 8) coupled to a local memory bus (Figure 1, Reference 10), the local memory bus separate from the system memory bus (Figure 1, Reference 5), the memory element to be addressable via the system memory bus (it is evident from Figure 1 that a device coupled to system memory bus access the memory element via the system memory bus as this is the only interface to the memory element); an on-board processor having an arbiter to arbitrate the system memory bus, including monitoring the system memory bus for a reserved memory address (memory address corresponding to the local memory) and issuing a control signal (refer to abstract, the CPU arbitrates the system memory bus by selectively coupling the main memory bus (Ref. 9) or the local memory bus (Ref. 10) to the system memory bus via a signaling mechanism [digital devices communicate via signals and thus it is evident that the arbitration

mechanism in the processor communicates to the switch mechanism (ref. 6) that is should connect either bus 9 or 10 to bus 5 via a signal]); a switch (Figure 1, Reference 6) coupled to the local memory bus, the on-board processor and the system memory bus to receive the control signal and selectively switch the local memory bus, in response to the control signal, to the on-board processor to switch control of the memory element to the on-board processor and to the system memory bus to switch control of the memory elements to the host system [host system comprised of References 2, 3 and 4](Abstract).

Regarding claim 48, the on-board processor performs processing (read/write) on data from the memory element when the local bus is connected to the on-board processor.

Regarding claims 51, 54-56 and 59-60, Maruyama discloses initializing a circuit coupled to a host system bus, the circuit having reserved memory locations (addresses corresponding to local memory, Reference 8) and control logic (Figure 1, Reference 1), the reserved memory locations coupled to the control logic via an internal bus (the local memory (Ref. 8); monitoring the host system bus for a signal (signal is comprised of the address bits corresponding to an address of the local memory) indicating an address of one or more of the reserved memory locations (the local memory is used in common with an address space allocated to the main memory and thus in controlling the switch (Ref. 6), the control logic must determine which address correlates to the main memory and the local memory); and selectively coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus (Abstract; when host system, comprised of devices 2, 3 or 4, access local memory by one of its components

the local memory is coupled to the system bus) or to the control logic to switch control of the indicated reserved memory location to the control logic, depending on whether the signal having the address is detected (Abstract; the switch couples the control logic [cpu] to the local memory when accessed by the control logic).

Regarding claims 52 and 57, Maruyama discloses coupling the internal bus to the host system bus to switch control of the indicated reserved memory location to the host system bus if the address comprises a first address (first address is an address requested by the host system which corresponds to the local memory); coupling the internal bus to control logic to switch control of the indicated reserved memory location to the control logic if the address comprises a second address (second address is an addresses requested by the control logic which corresponds to the local memory).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (JP-05120128).

Maruyama discloses the limitations cited above in claim 44, Maruyama does not disclose interconnecting the local memory bus to the host system via one of multiple system memory card

slots. However, it is well known in the art to store memory devices (such as the local memory in Maruyama) in a memory card slot on a printed circuit board to interface to the system bus. This provides an easy interface to connect external devices to the system bus. Thus, it would have been obvious to one of ordinary skill in the art to implement this feature in the system taught by Maruyama for the desirable purpose of providing a simple interface mechanism.

Response to Arguments

6. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

7. Claims 46, 49-50, 53 and 58 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jun et al. – USPN : 6,421,343- arbitrating access to a local memory bus

Fowler – USPN: 6,052,129 – arbitrating access to a local memory bus

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on Tues, Thr, Fri (10:00 - 6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

March 19, 2005